BOWEN UNIVERSITY IWO, OSUN STATE
COLLEGE OF COMPUTING AND COMMUNICATION STUDIES
COMPUTER SCIENCE PROGRAMME
B. SC. DEGREE SECOND SEMESTER EXAMINATION SESSION: 2022/2023
COURSE TITLE: COMPUTER ARCHITECTURE AND ORGANIZATION II
COURSE CODE: CIT 302 TIME ALLOWED: 2 HOURS CREDIT: 3 UNITS
INSTRUCTION: Answer any four (4) questions in all.

QUESTION 1

a) Determine the dependency relations among the following program instructions: **5 marks**

I_1: a = b
I_2: c = a + d
I_3: a = c

b) Consider a water bottle packaging plant. Let there be 3 stages that a bottle should pass through: Inserting the bottle(**I**), Filling water in the bottle(**F**), and sealing the bottle(**S**). Let us consider these stages as stage 1, stage 2 and stage 3 respectively. Let each stage take 1 minute to complete its operation.
Scenario 1: When the bottle is in stage 2, another bottle can be loaded at stage 1. Similarly, when the bottle is in stage 3, there can be one bottle each in stage 1 and stage 2. So, after each minute, we get a new bottle at the end of stage 3.
Scenario 2: A bottle is first inserted in the plant, after 1 minute it is moved to stage 2 where water is filled. Now, in stage 1, nothing is happening. Similarly, when the bottle moves to stage 3, both stage 1 and stage 2 are idle.

i. In your opinion, what Computer Architecture concept describes scenario 1 and scenario 2? **2 marks**
ii. Itemize four (4) differences between the two concepts. **6 marks**
iii. What is the average time to manufacture 1 bottle in both scenarios? **2 marks**
iv. Explain the five (5) classifications of scenario 1. **10 marks**

QUESTION 2

a) Define Control Unit of the CPU. Hence, itemize three (3) uses of control signal. **6 marks**
b) Briefly describe strobe method in asynchronous data transfer and state the advantages of asynchronous data transfer in computer organization. **8 marks**
c) State the major disadvantages of strobe method. **3 marks**
d) Compare and contrast hardwired and microprogrammed control units based on the following features: speed, modification, cost, handling complex instructions, instruction decoding, instruction set size, control memory and application. **8 marks**

QUESTION 3

a) Define reduced instruction set computers (RISC). Highlight the advantages of RISC based designs. **11 marks**
b) State the effect of using pipelining in RISC architecture operations. **3 marks**
c) RISC systems have been defined and designed in a variety of ways by different groups, list three (3) key elements shared by most designs. **3 marks**
d) Explain the four (4) main characteristics of reduced instruction set computers. **8 marks**

QUESTION 4

a) State the approach adopted in hardware fault tolerant techniques design. **5 marks**

b) Briefly describe fault masking as an approach in hardware fault tolerance recovery and give a specific solution for this. **6 marks**

c) Identify the symptoms of the semantic gap created due to the difference between the operations provided in HLLs and those provided in computer architecture. **6 marks**

d) Considering the behavior and performance of various high-level language programs' operations.

i. Which class of operation is the most time consuming? and **3 marks**

ii. Suggest a solution to minimize the time. **5 marks**

QUESTION 5

a) Different kinds of register are found within the CPU. Explain these registers. **6 marks**

b) Itemize four (4) examples of registers. **4 marks**

c) List five (5) differences between cache, memory and register. **5 marks**

d) With relevant example(s) and diagram, discuss the characteristics of registers, cache, main memory and disk memory (storage). **10 marks**

QUESTION 6

a) Define Memory Addressing Mode. **3 marks**

b) With appropriate diagram and example(s), list and discuss four (4) types of memory addressing mode. **10 marks**

c) In the diagram below, in cycle 4, instructions I_1 and I_4 are trying to access same resource (memory) which introduces a resource conflict.

Instruction / Cycle	1	2	3	4	5
I_1	IF(Mem)	ID	EX	Mem	
I_2		IF(Mem)	ID	EX	
I_3			IF(Mem)	ID	EX
I_4				IF(Mem)	ID

i. What computer architecture concept describes the above scenario? **2 marks**

ii. With a well labelled diagram, explain two (2) possible solutions to the resources conflict described in the above scenario. **10 marks**